Amendments to the Specification:

Please replace the paragraph beginning at page 27, line 1, with the following amended paragraph:

Fig. 17O ~~17P~~ shows a doping profile of two implants, with the deeper implant having a greater dose such that the peak concentration of the implants is approximately the same.

Please replace the paragraph beginning at page 27, line 6, with the following amended paragraph:

Fig. 17Q ~~17R~~ is a cross-sectional view showing a series of implants through a window in a photoresist layer, showing the lateral spreading of the implants in the substrate.

Please replace the paragraph beginning at page 27, line 8, with the following amended paragraph:

Fig. 17R ~~17S~~ is a cross-sectional view similar to that shown in **Fig. 17Q ~~17R~~**, except that the dopant is implanted into a region between two trenches filled with a nonconductive material to restrict the lateral spreading of the dopants.

Please replace the paragraph beginning at page 27, line 11, with the following amended paragraph:

Fig. 17S ~~17T~~ is a cross-sectional view similar to **Fig. 17R ~~17S~~**, except that the deepest dopant is implanted to a level below the two trenches, allowing it to spread laterally.

Please replace the paragraph beginning at page 27, line 13, with the following amended paragraph:

Fig. 17T ~~17U~~ is a cross-sectional view of the implanted region that results from the series of implants shown in **Fig. 17S ~~17T~~**.

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Please replace the paragraph beginning at page 27, line 15, with the following amended paragraph:

Fig. 17U ~~17V~~ is a view of a series of chained P-type implants performed through an N-type epitaxial layer to a P-type substrate.

Please replace the paragraph beginning at page 27, line 17, with the following amended paragraph:

Fig. 17V ~~17W~~ is a view of the doping profile obtained from the implants shown in **Fig. 17U ~~17V~~**.

Please replace the paragraph beginning at page 27, line 19, with the following amended paragraph:

Fig. 17W ~~17X~~ is a view of a series of chained implants similar to those shown in **Fig. 17U ~~17V~~** except that the implants are constrained by a pair of dielectric-filled trenches.

Please replace the paragraph beginning at page 27, line 21, with the following amended paragraph:

Fig. 17X ~~17Y~~ is a view of the doping profile obtained from the implants shown in **Fig. 17W ~~17X~~**.

Please replace the paragraph beginning at page 27, line 23, with the following amended paragraph:

Fig. 17Y ~~17Z~~ shows a CIJI sidewall isolation region comprising a series of implants into a P-substrate which overlaps onto a deep implanted N-type floor isolation region in an annular or ring pattern to form an isolated pocket separated from the common substrate.

Please replace the paragraph beginning at page 27, line 27, with the following amended paragraph:

Fig. 17Z ~~17AA~~ is a view of the doping profile obtained from the implants shown in **Fig. 17Y ~~17Z~~**.

Please replace the paragraph beginning at page 28, line 1, with the following amended paragraph:

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Fig. 17AA ~~**17BB**~~ illustrates the use of dielectric-filled trenches to constrain the lateral straggle of the implants shown in **Fig. 17Y** ~~**17Z**~~.

Please replace the paragraph beginning at page 28, line 3, with the following amended paragraph:

Fig. 17BB ~~**17CC**~~ is a view of the doping profile obtained from the implants shown in **Fig. 17AA** ~~**17CC**~~.

Please replace the paragraph beginning at page 28, line 5, with the following amended paragraph:

Figs. 18A-1 to **18A-4, 18B-1** to **18B-4**, and **18C-18H** ~~**Figs. 18A-18H**~~ are cross-sectional views of a "device arsenal" that can be fabricated simultaneously in a substrate using a process of this invention.

Please replace the paragraph beginning at page 28, line 7, with the following amended paragraph:

Fig. 18A-1 ~~**Fig. 18A**~~ shows a 5V PMOS and ~~PMOS,~~ a 5V NMOS~~, a 12V PMOS, a 12V NMOS, a 5V NPN, a 5V PNP, a 30V channel stop, and a 30V lateral trench DMOS~~.

Please replace the paragraph beginning at page 28, line 9, with the following amended paragraph:

Fig. 18B-1 ~~**Fig. 18B**~~ shows a 12V symmetrical isolated PMOS ~~CMOS, a poly-to-poly capacitor, an NPN with P-base, a 12V channel stop, and a 12V lateral trench DMOS~~.

Please replace the paragraph beginning at page 28, line 20, with the following amended paragraph:

Figs. 19A-19H are equivalent circuit diagrams of some of the devices shown in **Figs. 18A-1** to **18A-4, 18B-1** to **18B-4** and **18C-18H** ~~**Figs. 18A-18G**~~.

Please replace the paragraph beginning at page 28, line 22, with the following amended paragraph:

Fig. 19A shows the 5V CMOS shown in **Fig. 18A-1** ~~**Fig. 18A**~~.

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Please replace the paragraph beginning at page 28, line 23, with the following amended paragraph:

Fig. 19B shows the 12V CMOS shown in **Fig. 18A-2** ~~**Fig. 18A**~~.

Please replace the paragraph beginning at page 28, line 24, with the following amended paragraph:

Fig. 19C shows the 5V NPN shown in **Fig. 18A-3** ~~**Fig. 18A**~~.

Please replace the paragraph beginning at page 28, line 25, with the following amended paragraph:

Fig. 19D shows the 5V PNP shown in **Figs. 18A-3** and **18A-4** ~~**Fig. 18A**~~.

Please replace the paragraph beginning at page 28, line 26, with the following amended paragraph:

Fig. 19E shows the 30V trench lateral DMOS shown in **Fig. 18A-4** ~~**Fig. 18A**~~.

Please replace the paragraph beginning at page 29, line 1, with the following amended paragraph:

Fig. 19F shows the poly-to-poly capacitor shown in **Fig. 18B-2** ~~**Fig. 18B**~~.

Please replace the paragraph beginning at page 29, line 2, with the following amended paragraph:

Fig. 19G shows a poly resistor (not shown in **Figs. 18A-18H** ~~**Figs. 18A-18G**~~).

Please replace the paragraph beginning at page 29, line 6, with the following amended paragraph:

Figs. 21-67 illustrate the steps of a process for fabricating several of the devices shown in **Figs. 18A-1** to **18A-4, 18B-1** to **18B-4**, and **18C-18H** ~~**Figs. 18A-18G**~~, including the 5V CMOS, the 5V ~~the5V~~ NPN and 5V PNP (high F_T layout), the 5V ~~the5V~~ NPN and 5V PNP (conventional layout), the 30V lateral trench CMOS, and the symmetrical 12V CMOS. The letter suffix of each drawing number indicates the device to which it pertains, as follows:

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Please replace the paragraph beginning at page 29, line 11, with the following amended paragraph:

Suffix	Device
"A"	5V CMOS (**Fig. 18A-1** ~~**18A**~~)
"B"	5V NPN and 5V PNP (high F_T layout) (**Figs. 18A-3** and **18A-4** ~~**Fig. 18A**~~)
"C"	5V NPN and 5V PNP (conventional layout) (not shown)
"D"	30V lateral trench DMOS (**Fig. 18A-4** ~~**18A**~~)
"E"	Symmetrical 12V CMOS (**Figs. 18B-1** and **18B-2** ~~**Fig. 18B**~~)

Please replace the paragraph beginning at page 33, line 19, with the following amended paragraph:

Another feature of this invention is the ability to form fully isolated devices (including CMOS and bipolars of differing voltage) without the need for epitaxy. Such "epi-less" isolation combines a CIJI sidewall isolation structure in a ring, annular, or square donut-shape structure overlapping a deeply implanted floor isolation or buried dopant region having the same conductivity type as the CIJI sidewall isolation. Unlike devices made in epitaxial processes, the deep layers are not formed at the interface between a substrate and epitaxial layer, but by implanting the deep floor isolation dopant at high energies. An isolated pocket, having the same concentration and conductivity type as the original substrate, is the result of such a process. The content of such an isolated pocket may contain any number of doped regions of either P-type or N-type polarity including CMOS N well and P well regions, bipolar base regions, DMOS body regions, or heavily-doped source/drain ~~source-drain~~ regions. As used herein, the term "annular" refers to any structure that extends downward from the surface of the substrate and laterally surrounds an area of the substrate. Viewed from above, the annular structure may be circular (doughnut-shaped), or it may be oval, rectangular, polygonal, or any other shape.

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Please replace the paragraph beginning at page 35, line 1, with the following amended paragraph:

Initially, we describe a series of process steps by which N wells and P wells can be isolated from the substrate and from each other. For purposes of explanation, we assume the fabrication of a 5V N well, a 5V P well, a 12V N well, and a 12V P well. By "5V" and "12V" we refer to a well that is doped to a concentration and doping profile that allows the fabrication of a junction within the well that can withstand a reverse bias of the specified voltage and further that devices within the well will not leak or communicate with other devices so long as they are operated at the specified voltage level. In general, a 12V well is more lightly doped and deeper than a 5V well. In reality, a 5V well might be able to hold devices that can operate up to 7V, and a 12V well might be able to hold devices that can operate up to 15V. Thus "5V" and "12V" are somewhat arbitrary designations and generally used to describe the nominal voltage supply where such a device is meant to operate. ~~operate..~~

Please replace the paragraph beginning at page 39, line 23, with the following amended paragraph:

The 12V N-type guard ring is generally not self-aligned to field oxide 508. With misalignment, the guard ring may overlap into active areas 526 or 528 and adversely affect the electrical characteristics of devices produced in those regions. In extreme cases of misalignment, the guard ring can lower the breakdown voltage of the device produced in the N well ~~Nwell~~ below its 15V (12V operating) required rating. Even if guard ring 524 were somehow self-aligned to the field oxide region 508, implant 524 naturally diffuses laterally into the active areas 526 and 528 and may adversely affect the electrical characteristics of devices produced in those regions. To prevent this problem, the minimum dimension of field oxide 508 must then be increased, lowering the packing density of the devices.

Please replace the paragraph beginning at page 44, line 13, with the following amended paragraph:

Fig. 11G is a 12V version of a P well ~~Pwell~~ formed using a conventional process similar to that of the 5V version of **Fig. 11A**. To achieve sufficient field thresholds to prevent parasitic surface channels, guard ring 550 is formed under field oxide layer 536 prior to field oxidation. Accordingly, guard ring 550 diffuses laterally and must be spaced far away from active areas 546 and 548 to avoid adversely affecting devices fabricated in

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the active P wells ~~Pwell regions~~. Moreover, P well ~~the doping of Pwell~~ 544 must be more lightly doped than ~~that of~~ its 5V counterpart in **Fig. 11A**. In an attempt to reduce mask count, the same P well ~~Pwell~~ is sometimes used for both 5V and 12V devices. This compromise of under-doping the 5V P well ~~Pwell~~ can lead to many problems, especially in causing snapback and punchthrough breakdown effects in 5V NMOS. In some cases the minimum allowed channel length for N-channel devices must be lengthened to avoid these issues, but only by sacrificing packing density.

Please replace the paragraph beginning at page 48, line 1, with the following amended paragraph:

Figs. 13E and **13F** illustrate techniques of creating isolated pockets in accordance with the invention. A deep N layer DN is implanted at a high energy, typically 1.7 to 2.5 MeV phosphorus, at a dose ranging from 1E12 cm^{-2} to 5E15 cm^{-2} but preferably in the range of 9E13 cm^{-2}. Deep N layer DN is deeper in the active area 556 than under field oxide layer 552, but it does not touch the surface even under field oxide layer 552. To create a completely isolated pocket a sidewall isolation implant is necessary. The sidewall implant may be a dedicated ~~a dedicated~~ chained implant junction isolation (CIJI) or a stack of *as-implanted* well regions used in other devices within the IC. The sidewall, to obtain the highest concentration should preferably comprise a 5V N layer NW5B, as shown in **Fig. 13E**, or a combination of a 5V N layer NW5B and a 12V N layer NW12B, as shown in **Fig. 13F**. The deep N layer DN combined with the sidewall isolation isolates P-type pocket 554 from P-type substrate 500. The combined N-type isolation shell-like structure must be biased at a potential equal to or more positive than the substrate potential to avoid causing substrate injection problems. To achieve such a contact, the sidewall isolation requires some portion overlap onto an active (non-field oxide) area so as to allow electrical contact to the isolation structure (not shown).

Please replace the paragraph beginning at page 48, line 17, with the following amended paragraph:

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To minimize costs and maximize flexibility, it is preferable that the 5V N layer NW5B ~~MW5B~~ should be designed so that it overlaps the deep N layer DN, thereby eliminating the need for the 12V N layer NW12B to form the isolated pocket 554. If that event, the 12V N

layer NW12B does not need to be deposited in processes that do not contain 12V devices. In short, the 12V N layer NW12B ~~Nw12B~~ can be used when it is available, but it should not be necessary to form the pocket 554. This is an important feature of modularity, namely, the ability to eliminate all 12V process steps when 12V devices are not part of the structure.

Please replace the paragraph beginning at page 49, line 4, with the following amended paragraph:

Fig. 14A shows how a single deep N layer can be used to isolate complementary wells. 5V N well NW5 is similar to 5V N well NW5 in **Fig. 9B**, for example, and is surrounded by an 5V N layer NW5B. 5V P well PW5 and 5V P layer PW5B are similar but with reversed polarities, and where they meet at the surface the breakdown voltage will be adequate for 5V device ratings (typically from 8V to 12V). 5V N layer NW5B and 5V P layer PW5B are implanted with energies such that they contact the underside of field oxide layer 566. Deep N layer DN is similar to deep N layer DN shown in **Figs. 13E** ~~**Figs.13E**~~ and **13F** and is implanted with an energy such that it overlaps 5V N layer NW5B and 5V P layer PW5B. 5V N well NW5 is clearly isolated from P substrate 550 since any N well or DN region forms a reverse biased junction with the surrounding P-type substrate.. A portion of 5V N layer NW5B is allowed to pass through field oxide layer 566 on the right side of 5V P well PW5 in a ring or substantially annular shape so that 5V P well PW5 is likewise isolated from P substrate 500 because it is completely surrounded by N regions on all sides and beneath. 5V N well NW5 and 5V P well PW5 can float upward from the potential of P substrate 500, the limit being set by the distance L_D between a 5V P guard ring PW5B ~~well PW5 guard ring~~ and the 5V N layer NW5B ~~well NW5~~ on the right side of 5V P well PW5. For example, the complementary wells could hold 5V devices and float 30V above P substrate 500. With proper field shaping the maximum voltage of the floating region above the substrate could be extended to 60V, 200V or even 600V if it were desirable to do so. All of this is accomplished without any isolation diffusion or even a single epitaxial layer.

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Please replace the paragraph beginning at page 49, line 25, with the following amended paragraph:

The structure shown in **Fig. 14B** is similar to that shown in **Fig. 14A**, but here the deep N layer DN is restricted to the area under 5V P well PW5, and 5V P layer PW5B ~~well PW5~~ and 5V N layer NW5B ~~well NW5~~ are shown as touching. 5V N well NW5 is already isolated from P substrate 500. While the structures of **Fig. 14A** and **14B** have the same electrically equivalent circuit schematic, the quality of isolation of the deep N layer DN underlying NW5 is better than if it is not present, making the structure **Fig. 14A** preferred over its counterpart.

Please replace the paragraph beginning at page 50, line 1, with the following amended paragraph:

Fig. 14C shows a plan view of the structure of **Fig. 14A**, showing the distance L_D forming a drift region between the isolated structure and the surrounding 5V P guard ring PW5B ~~well PW5 guard ring~~. The dashed line represents the deep N layer DN, underlying both the Pwell and Nwell regions. The Pwell and the Nwell regions are shown touching, but could have a gap between them without causing any adverse affects. The Nwell NW5 (including its deep implanted portion NW5B) is shown to surround and circumscribe the Pwell region PW5 (which includes its subsurface portion PW5B). The shape of the entire isolated island can be rectangular as shown, but may include rounded corners to achive higher breakdown voltages.

Please replace the paragraph beginning at page 50, line 10, with the following amended paragraph:

Fig. 14D shows a plan view of an alternative embodiment wherein the grounded 5V P guard ring PW5B ~~well PW5 guard ring~~ touches the isolated structure (similar to Fig. 14C but with Ld = 0), and **Fig. 14E** shows a plan view of the structure of **Fig. 14B**, with the deep N layer DN (dashed line) being located only under (and slightly larger than) the 5V P well PW5.

Please replace the paragraph beginning at page 50, line 15, with the following amended paragraph:

Fig. 14F shows an N+ contact region 568 that is one means used to electrically bias the isolation structure (or shell) by contacting a portion of the 5V N well NW5 and the deep

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N layer DN through an opening in the field oxide layer 566. **Fig. 14G** illustrates one possible plan view of an N+ contact region 568 used to contact the shell-shaped N-type isolation structure. **Fig. 14H** shows an N+ contact region 570 that is used to contact a deep N layer DN and sidewall isolation that isolates a pocket 572 of P substrate 550. A deep N layer according to this invention can be used to isolate a 5V P well, a 5V N well, a 12V ~~a12V~~ P well, a 12V N well, and an isolated pocket of the P substrate 500. The more lightly doped P substrate pocket 572 can be used to integrate higher voltage or lower capacitance devices than those made inside P well regions PW5 or PW12.

Please replace the paragraph beginning at page 50, line 25, with the following amended paragraph:

Fig. 14I shows a deep N layer DN that extends around a 5V N well NW5 and toward the surface of P substrate 500, under the field oxide layer. In **Fig. 14J** the deep N layer DN is restricted to the area directly below the 5V N well NW5. While the N well ~~Nwell~~ overlaps onto the field oxide, the entire N well ~~Nwell~~ pocket is isolated by the artifact that it is opposite in conductivity type to the P-type substrate ~~substrates~~ that surrounds it. The entire island can float to a high voltage above the substrate, especially since the drift area L_{D2} ~~Ld_2~~ contains no well doping or field doping, either N-type or P-type. This structure and process sequence offer ~~offers~~ a distinct advantage over conventional junction isolation in that no additional masks are required to remove well or blanket field doping implants from this region.

Please replace the paragraph beginning at page 54, line 10, with the following amended paragraph:

Fig. 17A summarizes the conventional process of forming doped regions in a semiconductor material, which typically includes a masking step, a relatively shallow implant of dopant through openings in the mask, and a high temperature diffusion to diffuse or "drive in" the implanted dopant. Of course, there are normally steps preceding and following the introduction of dopant but they are not of primary ~~primarily~~ concern in this discussion (except that added diffusion affects, i.e. redistributes, dopants already present in the silicon at the time of the diffusion). In conventional CMOS and bipolar processes, shallow dopant layers are typically introduced by means of a single medium energy ion

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implantation, typically ranging from 60 keV to 130 keV. The implant is typically performed through a photoresist mask having a thickness of approximately 1 μm. Immediately post-implant, the dopant layer is, at most, only a few tenths of a micron in depth. The drive in diffusion is then performed using a high temperature process, ranging from 900 °C to 1150 °C over a period of 30 minutes to as much as 15 or 20 hours, but with 2 to 3 hours being common. Diffusion is often performed in nitrogen ambient, but oftentimes oxidation is performed during a portion of the diffusion cycle, leading to additional doping segregation effects and adding more variability in concentration and diffusion depth to the process. Final junction depths may range from 1 μm to 10 μm, with 1.5 μm to 3 μm junctions being common, except for the isolation and sinker diffusions ~~diffusion~~ discussed previously.

Please replace the paragraph beginning at page 57, line 13, with the following amended paragraph:

This effect can be counteracted, as shown in **Fig. 17O** ~~**17P**~~, by giving the deeper implant a dose Q_4 that is greater than the dose Q_3 of the shallower implant. As a result the straggle of the deeper implant ΔX_4 is greater than the straggle ΔX_3 of the shallower implant. **Fig. 17P** ~~**17Q**~~ illustrates the same principle with four implants having progressively higher doses Q_5, Q_6, Q_7 and Q_8, which yield almost a "flat" profile with a doping concentration of N_{13}. If it were desired to have the doping concentration slope upward with increasing depth, Q_6, Q_7 and Q_8 would have to be made progressively even higher.

Please replace the paragraph beginning at page 57, line 20, with the following amended paragraph:

As indicated above, the photoresist mask that is typically used to define the location of these chained implants is typically relatively thick, e.g., 3 μm to 5 μm thick. This makes it more difficult to achieve extremely small feature sizes using a small mask opening. Moreover, higher energy implants exhibit more lateral straggle from the implanted ions ricocheting off of atoms in the crystal and spreading laterally. So in fact, deeper implants spread more laterally than shallower lower-energy implants. That means unlike a Gaussian diffusion that is much wider at the top than at the bottom a chained implant stack is much more vertical in shape and is actually widest at the bottom, not the top. **Fig. 17Q** ~~**17R**~~

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shows a series of four implants through a window 700 in thick photoresist layer 702 and an oxide layer 704. Window 700 constrains the implants laterally, but window 700 cannot be made arbitrary small as the thickness of photoresist layer 702 is increased. In addition, the implanted dopant spreads laterally somewhat after it enters the substrate, especially at the higher energies and deeper depths.

Please replace the paragraph beginning at page 58, line 3, with the following amended paragraph:

A technique for constraining the implants to their smallest possible lateral extent is to form trenches in the semiconductor, as shown in **Fig. 17R** ~~**17S**~~. Trenches 706 can be filled with oxide or some other nonconductive material or with doped polysilicon. The implants overlap into the trenches 706, but have no effect there because the material filling the trenches 706 is nonconductive (or in the case of polysilicon, already heavily doped). The spacing W1 between trenches 706 can generally be made smaller than the width W2 of the opening 700 in the thick photoresist layer 702.

Please replace the paragraph beginning at page 58, line 10, with the following amended paragraph:

Moreover, as shown in **Fig. 17S** ~~**17T**~~ the dopant can be implanted at energies that propel it below the bottoms of trenches 706, producing a doped region 708 that has an inverted "mushroom" shape, as shown in **Fig. 17T** ~~**17U**~~, and a top edge that is below the surface of the semiconductor.

Please replace the paragraph beginning at page 58, line 14, with the following amended paragraph:

The chained implant described can comprise a chained implant junction isolation (CIJI) region that may be implanted into and through an epitaxial layer or used to overlap onto a deeply implanted buried implant of like conductivity type. For example in **Fig. 17U** ~~**17V**~~, an epitaxial layer 711 opposite in conductivity type to that of a substrate is isolated by a chain of implants 713a to 713f of the same conductivity type as the substrate (e.g. a boron chained isolation implant implanted into a P-substrate) implanted through a photolithographically-defined photoresist layer 712. The resulting isolation structure shown

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in **Fig. 17V** ~~**17W**~~ illustrates the resulting structure of CIJI structure 715 isolating epi layer 711.

Please replace the paragraph beginning at page 58, line 23, with the following amended paragraph:

In **Fig. 17W** ~~**17X**~~, a similar CIJI isolation structure is constrained during implant not only by photoresist 712, but also by trenches 720a and 720b, filled with a dielectric material such as oxide, oxy-nitride, or by polysilicon. The resulting isolation structure is shown in **Fig. 17X** ~~**17Y**~~. The depth of trenches 720a and 720b may range from 0.7 um to the depth of the epi layer itself, but preferably should extend roughly half to three-quarters the distance from the surface to the bottom of the epi layer 711 as a compromise between constraining the implant and facilitating the trench refill process.

Please replace the paragraph beginning at page 58, line 30, with the following amended paragraph:

In **Fig. 17Y** ~~**17Z**~~, a CIJI sidewall isolation, comprising implants 733a to 733d, into a P-substrate 730a, overlaps a deep implanted floor isolation region DN 732 in an annular or ring pattern to form an isolated pocket 730b that is separated from the substrate 730a. The resulting isolation structure including CIJI structure 740 is shown in **Fig. 17Z** ~~**17AA**~~.

Please replace the paragraph beginning at page 59, line 3, with the following amended paragraph:

In a structure similar to that of **Fig. 17Y** ~~**17Z**~~, the CIJI sidewall isolation structure of **Fig. 17AA** ~~**17BB**~~ illustrates the use of dielectric filled trenches 750a and 750b to constrain the lateral straggle of successive implants 733a to 733e. The deepest implants (for example deep implant 733a ~~733e~~) overlap a deep isolation region DN 732 to isolate pocket 730b from P substrate 730a. The resulting structure with CIJI sidewall isolation 751 is illustrated in **Fig. 17BB** ~~**17CC**~~. The depth of trenches 750a and 750b may range from 0.7 um to the depth of the DN layer itself, but preferably should extend roughly half to three-quarters the distance from the surface to the deep DN layer 732 as a compromise between constraining the implant and facilitating the trench refill process.

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Please replace the paragraph beginning at page 59, line 18, with the following amended paragraph:

Figs. 18A-1 to **18A-4, 18B-1** to **18B-4** and **18C-18H** ~~**Figs. 18A-18H**~~ show a family of devices that can be fabricated by a process according to this invention. The process is performed on a single semiconductor chip, represented by a substrate 350, which is generally doped with a P-type impurity such as boron. The devices, and some of the regions within the devices, are separated laterally by a field oxide layer 352, which is grown at the surface of substrate 350 by a conventional local oxidation of silicon (LOCOS) process.

Please replace the paragraph beginning at page 59, line 24, with the following amended paragraph:

Starting with **Fig. 18A-1** ~~**18A**~~, the family of devices includes a 5V complementary MOSFET pair (CMOS) comprising a P-channel MOSFET (PMOS) 301 and an N-channel MOSFET (NMOS) 302.

Please replace the paragraph beginning at page 59, line 27, with the following amended paragraph:

PMOS 301 is formed in an N well 354A that serves as the body of PMOS 301. N well 354A includes shallow regions 356 that are formed by implanting dopant through field oxide layer 352, as described below. A gate 358A is formed above substrate 350, typically made of polycrystalline silicon (polysilicon) that may be capped with a metal layer. Gate 358A is bordered by sidewall spacers 360 and is separated from N well 354A by a gate oxide layer (not shown). The thickness of the gate oxide layer may range from 100A to 2000A but typically is in the range of 200A to 600A. Lightly-doped P drift regions 362A and 362B are formed in N well 354A on the sides of gate 358A. PMOS 301 also includes a P+ source region 364A and a P+ drain region 364B. (Throughout **Figs. 18A-1** to **18A-4, 18B-1** to **18B-4**, and **18C-18H** ~~**Figs. 18A-18H**~~ dopant regions designated by the same reference numeral but different letter are formed during the same implant step.)

Please replace the paragraph beginning at page 60, line 18, with the following amended paragraph:

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Referring to **Fig. 18A-2**, substrate ~~Substrate~~ 350 also contains a 12V PMOS 303 and a 12V NMOS 304. 12 V PMOS 303 is formed in an N well 380A, which is implanted with dopant at a higher energy than N well 354A in PMOS 301. A gate 358C is formed from the same polysilicon layer as gates 358A, 358B, but the gate oxide layer that separates gate 358C from the substrate is typically thicker than the gate oxide layers beneath gates 358A, 358B. A minimum gate oxide thickness to sustain continuous operation at 12V should preferably meet or exceed 300A. The source is formed by a P+ region 364C and the drain is formed by a P+ region 364D. The drain is offset from the edge of gate 358C by a distance that is not determined by a sidewall spacer on gate 358C. Instead, as described below, P+ drain 364D is formed in a separate masking step. A lightly-doped P region 363B extends between the drain region 364D and the gate 358C and likewise between the drain and field oxide 352. On the other hand, the P+ source 364C of 12V PMOS 303 is aligned with a sidewall spacer 360 on gate 358C. Thus 12V PMOS 303 is not a symmetrical device. The drain 364D is offset by a considerable margin (e.g., 0.3-1.0 μm) from the edge of gate 358C, whereas the source 364C is offset by only a small margin (e.g., 0.15 μm).

Please replace the paragraph beginning at page 61, line 23, with the following amended paragraph:

Referring to **Fig. 18A-3**, a A 5V NPN bipolar transistor (NPN) 305 includes a double P well 372C as a base. Double P well 372C is formed during the same implant as P well 372A in NMOS 302. The use of a double P well allows the base to be contacted at a remote location through a P+ region 364E. Double P well 372C is relatively shallow (e.g., 0.5- 1.0 μm deep), which is typical of junction depths used for bipolar transistors in prior art processes. An N+ region 378E acts as an emitter, which can be made very small, reducing the sidewall capacitance of the emitter to base. The collector of 5V NPN 305 includes an N well 354C, which merges with a deep N (DN) layer 390A.

Please replace the paragraph beginning at page 62, line 12, with the following amended paragraph:

Referring to **Figs. 18A-3 and 18A-4**, a 5V PNP bipolar transistor (PNP) 306 has a wraparound "floor isolation" and sidewall isolation region that includes a 5V N well 354E

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and a deep N layer 390B. N well 354E is contacted through an N+ region 378H and can be biased at the collector voltage or at the most positive voltage on the chip, in which case the collector-to-"floor" junction would be either zero-biased or reverse-biased. The emitter of PNP 306 is a P+ region 364G. The collector includes a 12V P well 386B, which actually consists of three wells that merge together, and a 5V P well 372D, which is used as an additional collector sinker to reduce the resistance. The base includes a dedicated N base region 394 and is contacted through a 5V N well 354D and an N+ contact region 378G. Alternatively, the section of field oxide layer 352 between the emitter and base can be removed, in which case the N implant 394 will extend under the base contact and the emitter capacitance will increase.

Please replace the paragraph beginning at page 62, line 24, with the following amended paragraph:

Referring to **Fig. 18A-4**, a 30V channel stop 307 includes a non-contacted P+ region 364H, which sits over a 12V P well 386C and a 5V P well 372E. This not only prevents surface inversion, but if any minority carriers attempt to flow laterally, they can be collected.

Please replace the paragraph beginning at page 63, line 13, with the following amended paragraph:

To summarize, **Figs. 18A-1** to **18A-4** show ~~**Fig. 18A** shows~~ a group of devices that include fully optimized 5V and 12V CMOS pairs (301, 302 and 303, 304), complementary bipolar transistors (305, 306) and a 30V lateral trench DMOS (308), all formed in a single chip, with no epitaxial layer and in a single process with no long diffusions. The bipolar transistors (305, 306) are fully isolated from the substrate 350, but it should be understood that the CMOS pairs (301, 302 and 303, 304) can similarly be isolated by adding the deep N layer 390 under them.

Please replace the paragraph beginning at page 63, line 20, with the following amended paragraph:

Figs. 18B-1 to **18B-4** show ~~**Fig. 18B** shows~~ a second group of devices that can be formed in the same process, including a 12V symmetrical isolated CMOS pair 309, 310, a

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poly-to-poly capacitor 311, an NPN 312, a 12V channel stop 313 and a 12V lateral trench DMOS 314.

Please replace the paragraph beginning at page 63, line 23, with the following amended paragraph:

Referring to **Figs. 18B-1** and **18B-2**, a 12V symmetrical isolated CMOS pair 309, 310 is isolated from substrate 350 by a deep N layer 390C which merges with a 12V N well 380C. Within N well 380C is a 5V N well 354H, contacted by N+ and metal (not shown). PMOS 309 is isolated from substrate 350 so long as the potential of N well 380C is higher than the potential of substrate 350. NMOS 310 is isolated from substrate 350 because it is surrounded by N-type material.

Please replace the paragraph beginning at page 64, line 25, with the following amended paragraph:

Referring to **Fig. 18B-3**, an NPN 312 has a base which includes a P base region 395B (which is formed with a specific mask), an isolated region 392B of substrate 350, and a P+ base contact region 364L. The emitter of NPN 312 is an N region 378L. The collector is an N isolation region 354K, which merges with a deep N layer 390D. Unlike NPN 305 in **Fig. 18A-3** ~~**Fig. 18A**~~, which has a section of field oxide layer 352 between the base and the emitter and N well 372C underlying the field oxide layer 352, in NPN 312 the entire area is active and no N well is necessary. As a result, the base-to-emitter capacitance of NPN 312 is greater than the base-to-emitter capacitance of NPN 305.

Please replace the paragraph beginning at page 65, line 10, with the following amended paragraph:

Referring to **Fig. 18B-4**, a 12V channel stop 313 includes a 5V P well 372G and a 12V P well 386E, which are contacted via a P+ region 364M. P+ region 364M extends on opposite sides of a trench gate 396B, which is optional. The function of 12V channel stop 313 is to prevent the surface of substrate 350 from being inverted by any overlying metal lines biased at high voltages.

Please replace the paragraph beginning at page 65, line 15, with the following amended paragraph:

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12V lateral trench DMOS 314 is essentially a smaller version of 30V lateral trench DMOS 308 in **Fig. 18A-4** ~~**18A**~~. 12V DMOS 314 includes a trench which is filled with a polysilicon gate 396C and lined with a gate oxide layer 398C. Lateral trench DMOS 314 also includes a drain consisting of a 5V N well 354L, an N+ contact region 378N and a dedicated lightly-doped N drift region, which includes a shallower portion 391B under field oxide layer 352 and a deeper drift portion 393B. A P body region 395C, which is a dedicated implant, is contacted through a P+ body contact region 364N. The source is represented by N+ regions 378P which are adjacent the trench. The current flows from N+ source regions 378P downward through a channel within P body region 395C and then turns and flows laterally towards 5V N well 354L and N+ contact region 378N. Gate 396C acts as a lateral current-spreader to spread the current in the high-voltage N drift region and thereby reduce the current density and resistance within that area.

Please replace the paragraph beginning at page 66, line 1, with the following amended paragraph:

Referring to **Fig. 18C**, the device family includes a fully isolated 5V CMOS pair consisting of a 5V NMOS 315 and a 5V PMOS 316. NMOS 315 includes an N+ source region 378R and an N+ drain region 378S formed in a 5V P well 372H, which also includes a P+ body contact region 364P (shown as a butting contact to N+ region 378R). A gate 358H overlies a channel in P well 372H. NMOS 315 is isolated from substrate 350 by an underlying deep N layer 390E, which merges with an N-type sidewall isolation region 354N and an N+ contact region 378Q. In such device the wrap-around isolation may be biased to a different potential than the NMOS source and body, which still may be shorted locally by the butting contact. As described above, the NMOS may have a sidewall spacer with an underlying LDD (similar to an isolated version of NMOS 302 in **Fig. 18A-1** ~~**18A**~~) or in simpler versions of the process, the sidewall spacer and shallow LDD implant may be omitted.

Please replace the paragraph beginning at page 66, line 13, with the following amended paragraph:

PMOS 316 includes a P+ drain region 364Q and a P+ source region 364R formed in a 5V N well 354P, which also includes an N+ body contact region 378T. A gate 358I

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overlies a channel in N well 354P. PMOS 316 is isolated from the substrate 350 as an artifact of its construction in an N well 354P, but may be further isolated from substrate 350 by extending deep N layer DN 390E under the N well to reduce any parasitic bipolar gain to the substrate. Electrical contact to substrate 350 is made via a P+ contact region 364S and a 5V P well 372I. As described above, the PMOS may have a sidewall spacer with an underlying LDD (similar to an isolated version of PMOS 301 in **Fig. 18A-1** ~~**18A**~~) or in simpler versions of the process, the sidewall spacer and shallow LDD implant may be omitted. A butting contact between the P+ source 364R and the N+ body contact 378T illustrates a fully isolated PMOS can still employ local source to body shorts.

Please replace the paragraph beginning at page 68, line 4, with the following amended paragraph:

Fig. 18H shows a lateral P-channel DMOS 400 that includes a gate 358K, an P+ source region 364W, an P+ drain region 364V, and an N well (acting as a DMOS body) 354S ~~354R~~ that is contacted via a N+ body contact region 378X. Current flows from P+ source region 364W through a channel in N well 354S ~~354R~~ (located under a gate oxide beneath the polysilicon gate 358K) and through a high-voltage drift region 401 (which is simply the isolated portion of P substrate 350) and (optionally into a 5V P well) to P+ drain region 364V.

Please replace the paragraph beginning at page 68, line 11, with the following amended paragraph:

To summarize, the entire family of devices described above can be fabricated on a single substrate 350 using a series of 11 basic implants, identified as follows in **Figs. 18A-1 to 18A-4, 18B-1 to 18B-4 and 18C-18H** ~~**18A-18H**~~ and in Table 1 (without the letter suffixes).

Please replace the paragraph beginning at page 69, line 8, with the following amended paragraph:

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Figs. 19A-19H are equivalent circuit diagrams of some of the devices shown in **Figs. 18A-1 to 18A-4, 18B-1 to 18B-4 and 18C-18H** ~~**18A-18H**~~. In **Figs. 19A-19H,** "S" represents the source, "D" represents the drain, "G" represents the gate, "B" represents

the body or base, "C" represents the collector, "E" represents the emitter, "DN" represents a deep N layer, and FI represents the floor isolation connection (when applicable).

Please replace the paragraph beginning at page 70, line 7, with the following amended paragraph:

Fig. 19H shows a conventional 30V lateral DMOS 320 whose source and body terminals are shorted together and tied to the substrate and whose drain terminal is isolated from the substrate by a diode D9. Schematically the N-channel lateral (surface) DMOS 320 shown in **Fig. 18G** and the N-channel trench lateral DMOS 308 shown in **Fig. 18A-4** ~~**18A**~~ appear to have identical schematics, but their construction is completely different. We include them both in the schematic to highlight their difference (one is a surface conduction device, the other one conducts in a channel vertically down a trench sidewall).

Please replace the paragraph beginning at page 70, line 15, with the following amended paragraph:

Figs. 20A and **20B** provide an overview of an illustrative process according to this invention that can be used to fabricate the devices shown in **Figs. 18A-1 to 18A-4, 18B-1 to 18B-4 and 18C-18H** ~~**18A-18G**~~. The process is depicted as a sequence of "cards" that briefly summarizes the steps of the process. Cards that have clipped corners represent optional process steps. The process is described in greater detail below in the description of **Figs. 21-67**.

Please replace the paragraph beginning at page 71, line 3, with the following amended paragraph:

Figs. 21-67 illustrate a process for fabricating several of the devices shown in **Figs. 18A-1 to 18A-4, 18B-1 to 18B-4 and 18C-18H** ~~**18A-18H**~~: in particular the 5V PMOS 301, 5V NMOS 302, 5V NPN 305, 5V PNP 306, 30V lateral trench DMOS 308, 12V PMOS 309, and 12V NMOS 310. The 5V NPN 305 are 5V PNP 306 are shown both in a conventional form and in a form which provide high-speed operation (high f_T). The process uses a single substrate 350.

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Please replace the paragraph beginning at page 72, line 22, with the following amended paragraph:

As shown in **Fig. 25D**, in the area that will contain 30V Lateral Trench DMOS 308, a nitride layer 410, a TEOS oxide layer 412, and a photoresist mask layer 414 are deposited in succession on top of pad oxide layer 408. Nitride layer 410 can be in the range of 0.1 to 0.6 μm thick but typically 0.2 μm. TEOS oxide layer 412 is deposited by the well known process and can be 200A to 2 um thick, for example, but typically has a thickness of 700A. Photoresist mask layer 414 is photolithographically patterned by forming relatively narrow openings 415, which are then used to etch through TEOS oxide layer 412 and nitride layer 410 and into substrate 350, forming trenches 416 in substrate 350. Preferably, a directional process such as reactive ion etch (RIE) is used to etch into substrate 350. Trenches 416 can be typically 0.5 μm wide (but can range from 0.25 μm to 1 um) and between 0.8 to 2 μm (typically 1.5 μm) deep, for example. (Note that four trenches 416 are shown in **Fig. 25D**, whereas only a single trench for 30V lateral trench DMOS 308 is shown in **Fig. 18A-4** ~~**18A**~~. It will be understood by those skilled in the art that lateral trench DMOS 308 could have any number of trenches while the basic structure of lateral trench DMOS 308 remains the same.)

Please replace the paragraph beginning at page 73, line 30, with the following amended paragraph:

A photoresist mask (not shown) is formed over interlayer dielectric 387, and interlayer dielectric 387 and polysilicon layer 389 are removed except in the areas where the photoresist mask remains. One of the areas where the photoresist mask remains is the portion of substrate 350 where poly-to-poly capacitor 311 is to be formed. As shown in **Fig. 18B-2** ~~**18B**~~, polysilicon layer 389 forms the bottom plate and interlayer dielectric 387 forms the dielectric layer of poly-to-poly capacitor 311. After poly-to-poly capacitor 311 has been formed the photoresist mask (not shown) is removed.

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Please replace the paragraph beginning at page 74, line 15, with the following amended paragraph:

As shown in **Figs. 35A-35E**, a photoresist mask layer 430 is deposited and photolithographically patterned to form openings in all areas except where the illustrated

lateral trench DMOS is to be formed (**Fig. 35D**). Other trench DMOS variants which use a deep N (DN) layer in part of their structure would in fact also be masked and patterned to receive the implant. An N-type dopant is implanted through the openings in mask layer 430 to form the deep N (DN) layers. In the areas of the 5V PNP and 5V NPN (both the high f_T and conventional layouts) deep N layers 390A and 390B are formed (**Fig. 35B** and **35C**). In the area of the symmetrical 12V CMOS, deep N layer 390C is formed (**Fig. 35E**). In the area of 5V NMOS 302, a deep N layer 390G is formed. (Note that this is a variation from the embodiment shown in **Fig. 18A-1** ~~**18A**~~, where 5V NMOS 302 has no underlying deep N layer and is thus not isolated from substrate 350.) Deep N layer 390 could be formed, for example, by implanting phosphorus at a dose of 1E13 to 5E14 cm^{-2} but typically at a dose of 5E13 cm^{-2} and an energy of 1.5 MeV to 3 MeV but typically at 2.0 MeV. This would produce a deep N layer having a doping concentration of approximately 1E18 cm^{-3} and a range of 2 to 3 μm below the surface of substrate 350 and a straggle of 0.3 μm. At 2 MeV, the thickness of the isolated P substrate above the DN layer without the addition of a P well is approximately 1 μm.

Please replace the paragraph beginning at page 82, line 6, with the following amended paragraph:

As shown in **Figs. 65A-65E**, a photoresist mask layer 484 is deposited and photolithographically patterned with openings over certain of the openings in interlayer dielectric 480. An N-type dopant is implanted through the openings in mask layer 484 to form "N-plug" regions. The N-plug regions are heavily doped and improve the ohmic contact between the metal layer to be deposited later and the N-type regions of substrate 350. Note that since the N-type dopant enters the N+ regions previously formed the N-plug regions are not visible in **Figs. 18A-1 to 18A-4, 18B-1 to 18B-4,** ~~**18A, 18B**~~ or **65A-65E**. The N-plug implant could be phosphorus or arsenic at a dose of 6E19 cm^{-2} and an energy of 30 keV, yielding shallow N-plug regions of nearly degenerate doping. Mask layer 484 is removed.

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Please add the following new paragraphs after the paragraph ending at page 28, line 8:

Fig. 18A-2 shows a 12V PMOS and a 12V NMOS.

Fig. 18A-3 shows 5V NPN and a portion of a 5V PNP.

Fig. 18A-4 shows the remaining portion of the 5V PNP, a 30V channel stop and a 30V lateral trench DMOS.

Please add the following new paragraphs after the paragraph ending at page 28, line 10:

Fig. 18B-2 shows a 12V symmetrical isolated NMOS and a poly-to-poly capacitor.

Fig. 18B-3 shows an NPN with P-base mask (not standard).

Fig. 18B-4 shows a 12V channel stop and a 12V lateral trench DMOS.

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